Amendments to the Claims:

Please amend the claims as follows:

Claim 1 (Original): A semiconductor device, comprising:

a workpiece including a first region and a second region;

a sensor formed in the first region;

at least one first insulating layer disposed over the sensor in the first region and disposed over the second region;

a plurality of apertures formed in each at least one insulating layer over the sensor; and

a second insulating layer disposed over the at least one first insulating layer and the plurality of apertures in the at least one first insulating layer, wherein each aperture forms a hollow region beneath the second insulating layer within the at least one first insulating layer.

Claim 2 (Original): The semiconductor device according to Claim 1, further comprising interconnects formed in the at least one first insulating layer in the second region of the workpiece.

Claim 3 (Original): The semiconductor device according to Claim 1, wherein the at least one first insulating layer comprises a first thickness, wherein each aperture extends through the first thickness of the at least one first insulating layer.

Claim 4 (Original): The semiconductor device according to Claim 3, wherein the at least one insulating layer comprises a plurality of inter-metal dielectric (IMD) layers, the plurality of IMD layers comprising a second thickness, wherein metal interconnects are formed within the plurality of IMD layers, and wherein each aperture extends through the second thickness of the IMD layers.

Claim 5 (Currently amended): The semiconductor device according to Claim 4, wherein the at least one insulating layer comprises an inter-layer dielectric (ILD) layer disposed over and abutting the workpiece, the ILD ~~at least one insulating~~layer comprising a third thickness, and wherein each aperture extends through the third thickness of the ILD layer and the second thickness of the plurality of IMD layers.

Claim 6 (Original): The semiconductor device according to Claim 5, wherein the ILD layer comprises about 4,000 Å to about 10,000 Å of SiO_2, fluorinated silicate glass (FSG) oxide, plasma-enhanced oxide, high density plasma (HDP) oxide, or spin-on glass (SOG).

Claim 7 (Original): The semiconductor device according to Claim 5, further comprising a layer of silicon nitride or silicon oxynitride disposed between the sensor and the ILD layer, the silicon nitride or silicon oxynitride layer comprising a fourth thickness, wherein each aperture extends through the fourth thickness of the silicon nitride or silicon oxynitride layer.

Claim 8 (Original): The semiconductor device according to Claim 5, further comprising a layer of silicon nitride or silicon oxynitride disposed between the sensor and the ILD layer, the silicon nitride or silicon oxynitride layer comprising a fourth thickness, wherein each aperture does not extend through the fourth thickness of the silicon nitride or silicon oxynitride layer.

Claim 9 (Original): The semiconductor device according to Claim 4, wherein the plurality of IMD layers comprise a plurality of layers comprising SiN, SiON, SiO_2, fluorinated silicate glass (FSG) oxide, plasma-enhanced oxide, high density plasma (HDP) oxide, spin-on glass (SOG), or combinations thereof.

Claim 10 (Original): The semiconductor device according to Claim 4, wherein each IMD layer comprises a barrier layer and an insulating layer disposed over the barrier layer.

Claim 11 (Original): The semiconductor device according to Claim 10, wherein each IMD layer insulating layer comprises about 6,000 Å to about 11,000 Å of SiO_2, fluorinated silicate glass (FSG) oxide, plasma-enhanced oxide, high density plasma (HDP) oxide, or spin-on glass (SOG), and wherein each IMD layer barrier layer comprises about 100 Å to about 800 Å of SiN or SiON.

Claim 12 (Original): The semiconductor device according to Claim 1, wherein each aperture comprises a shape of a circle, oval, square, rectangle, or a combination thereof.

Claim 13 (Original): The semiconductor device according to Claim 1, wherein each aperture comprises a width of about 1.0 μm or less.

Claim 14 (Original): The semiconductor device according to Claim 1, wherein the plurality of apertures are spaced apart by at least about 0.1 μm.

Claim 15 (Original): The semiconductor device according to Claim 1, wherein the second insulating layer comprises a non-conformal dielectric material.

Claim 16 (Original): The semiconductor device according to Claim 1, wherein the second insulating layer comprises a transparent or a translucent material.

Claim 17 (Original): The semiconductor device according to Claim 1, wherein the second insulating layer comprises about 4000 Å to about 8000 Å of plasma enhanced (PE) oxide, silicon nitride (SiN) or silicon oxynitride (SiON).

Claim 18 (Original): The semiconductor device according to Claim 1, wherein each aperture comprises a top region, wherein the second insulating layer extends into the top region of each of the plurality of apertures.

Claim 19 (Original): The semiconductor device according to Claim 1, wherein the sensor comprises a photodiode.

Claims 20–38 (Canceled).

Claim 39 (Original): A semiconductor device, comprising:

a workpiece including a first region and a second region;

a sensor formed in the first region;

at least one first insulating layer disposed over the sensor in the first region and disposed over the second region, the at least one first insulating layer comprising a

thickness;

interconnects disposed in the at least one first insulating layer in the second region of the workpiece;

a plurality of apertures formed in each at least one insulating layer over the sensor in the first region, each aperture extending through the thickness of the at least one first insulating layer; and

a second insulating layer disposed over the at least one first insulating layer and the plurality of apertures in the at least one first insulating layer, the second insulating layer comprising a non-conformal dielectric material, wherein each aperture forms a hollow region beneath the second insulating layer within the at least one first insulating layer.

Claim 40 (Original): The semiconductor device according to Claim 39, wherein the at least one first insulating layer comprises SiN, SiON, SiO_2, fluorinated silicate glass (FSG) oxide, plasma-enhanced oxide, high density plasma (HDP) oxide, spin-on glass (SOG), or combinations thereof, and wherein the second insulating layer comprises plasma-enhanced oxide, SiN or SiON.

Claim 41 (Original): The semiconductor device according to Claim 39, wherein the second insulating layer comprises a transparent or a translucent material.

Claim 42 (Original): The semiconductor device according to Claim 39, wherein each aperture comprises a top region, wherein the second insulating layer extends into the top region of each of the plurality of apertures.